REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

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1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
		01 Feb 2004 - 31 Jul 2006 FINAL

4. TITLE AND SUBTITLE
(THEME 3) ATOMICALLY SMOOTH EPITAXIAL FERROELECTRIC THIN FILMS FOR THE DEVELOPMENT OF A NONVOLATILE, ULTRAHIGH DENSITY, FAST, LOW VOLTAGE, RADIATION-HARD MEMORY

5. FUNDING NUMBERS
61102F
2305/TC

FA 9550-04-1-0061

6. AUTHOR(S)
DR AHN

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
YALE UNIVERSITY
GRANT AND CONTRACT ADMIN
155 WHITNEY AVENUE ROOM 214
NEW HAVEN CT 06520-8337

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AFOSR/NE
4015 WILSON BLVD
SUITE 713
ARLINGTON VA 22203
Dr Harold Weinstock

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
[redacted]

11. SUPPLEMENTARY NOTES
AFRL-SR-AR-TR-06-0396

12a. DISTRIBUTION AVAILABILITY STATEMENT
DISTRIBUTION STATEMENT A: Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*
The goal of this research is to fabricate atomically smooth, single crystalline, complex oxide thin film nanostructures for use in a nonvolatile, ultrahigh density, fast, low voltage, radiation-hard memory. For this work, we use complex oxide materials, which possess rich electronic phase diagrams, encompassing metallic, insulating, antiferromagnetic, and ferromagnetic behavior. Complex oxides can also exhibit ferroelectricity, which is characterized by the presence of a non-volatile spontaneous polarization field that is reversible by application of an external electric field. This switchable, bi-stable polarization field is the basis for the nonvolatile memory studied in this work. Advanced physical vapor deposition techniques, such as off-axis magnetron sputtering, are used to integrate the rich functionalities of complex oxides with the ferroelectrics used in this work. For this project, we use the ferroelectric perovskite, pbZr1-xTixO3 (PZT), with the bi-stable spontaneous polarization field of PZT being used to tune the electronic behavior of all-complex oxide field effect structures.

14. SUBJECT TERMS			15. NUMBER OF PAGES
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

Final Report for AFOSR project FA9550-04-1-0061 (Atomically Smooth Epitaxial Ferroelectric (Piezoelectric) Thin Films for the Development of a Nonvolatile, Ultrahigh Density, Fast, Low Voltage, Radiation-Hard Memory)

Summary:

The goal of this research is to fabricate atomically smooth, single crystalline, complex oxide thin film nanostructures for use in a nonvolatile, ultrahigh density, fast, low voltage, radiation-hard memory. For this work, we use complex oxide materials, which possess rich electronic phase diagrams, encompassing metallic, insulating, antiferromagnetic, and ferromagnetic behavior. Complex oxides can also exhibit ferroelectricity, which is characterized by the presence of a non-volatile spontaneous polarization field that is reversible by application of an external electric field. This switchable, bi-stable polarization field is the basis for the nonvolatile memory studied in this work. Advanced physical vapor deposition techniques, such as off-axis magnetron sputtering, are used to integrate the rich functionalities of complex oxides with the ferroelectrics used in this work. For this project, we use the ferroelectric perovskite, $PbZr_{1-x}Ti_xO_3$ (PZT), with the bi-stable spontaneous polarization field of PZT being used to tune the electronic behavior of all-complex oxide field effect structures.

The principal materials used for the conducting channels of the field effect structures are the correlated oxides $La_{1-x}Sr_xMnO_3$, $La_{1-x}Ca_xMnO_3$, and $La_{1-x}Sr_xCoO_3$. Films with high surface quality and crystallinity were grown and characterized. Ferroelectric / oxide bi-layer structures were fabricated and patterned into field effect devices. Electrical and magnetic properties were measured at room temperature and low temperature for the two polarization states of the ferroelectric layer. Studies of the resistance on/off ratio, retention, and switching speed of single devices were carried out. In addition, arrays of devices were fabricated that used a word line-bit line architecture to independently control the state of individual devices.

To integrate these oxide field effect devices with mainstream semiconductor technology, we also deposited crystalline oxide materials on silicon. An oxide molecular beam epitaxy (MBE) system was constructed for this purpose. Epitaxial $SrTiO_3$ thin films, which serve as buffer layers for the growth of ferroelectric oxides and correlated conducting oxides, were deposited on silicon wafers.

Characterization of single layer films:

Epitaxial $La_{1-x}Sr_xMnO_3$ (LSMO) thin films, with x = 0.16, 0.20, 0.33, and 0.35, $La_{1-x}Ca_xMnO_3$ (LCMO) with x = .20, 0.30, and 0.48, and $La_{0.70}Sr_{0.30}CoO_3$ (LSCO) were grown by RF magnetron sputtering on $SrTiO_3$ (STO), $NdGaO_3$ (NGO), and $LaAlO_3$ (LAO) substrates. Optimization of the growth conditions, such as

temperature and process gas pressure and composition, enabled us to deposit atomically smooth, 001-oriented films. For the complex oxide systems used, the x-ray diffraction rocking curves taken around the 001 reflection had a typical full width at half maximum of ~ 0.1° or less. Root-mean-square (RMS) roughnesses of 0.3 nm to 0.4 nm were achieved over micron-size length scales on LSCO, while LSMO and LCMO films had a typical RMS roughness of 0.1nm to 0.2nm, comparable to the roughness of the substrates used for growth.

Characterization of single devices:

$PbZr_{0.8}Ti_{0.2}O_3$ (PZT) / $La_{1-x}Sr_xMnO_3$ (LSMO), $PbZr_{0.8}Ti_{0.2}O_3$ (PZT) / $La_{0.70}Ca_{0.30}MnO_3$ (LCMO), and $PbZr_{0.8}Ti_{0.2}O_3$ (PZT) / $La_{0.70}Sr_{0.30}CoO_3$ (LSCO) heterostructures were fabricated, including single devices and four-device array configurations, using standard photolithographic processing. Ferroelectric field effect modulation of the transport properties of the LSMO layer was examined. In Figure 1, the resistivity as a function of temperature for a 4 nm $La_{0.84}Sr_{0.16}MnO_3$ layer is plotted for both polarization states of the ferroelectric layer. Applying a ±5 V, 100 μs pulse across the ferroelectric layer switches the structure between the on state and off states. In the on state, the resistivity peak temperature is ~190K, while in the off state the resistivity peak temperature is shifted downwards by ~30K to ~160K.

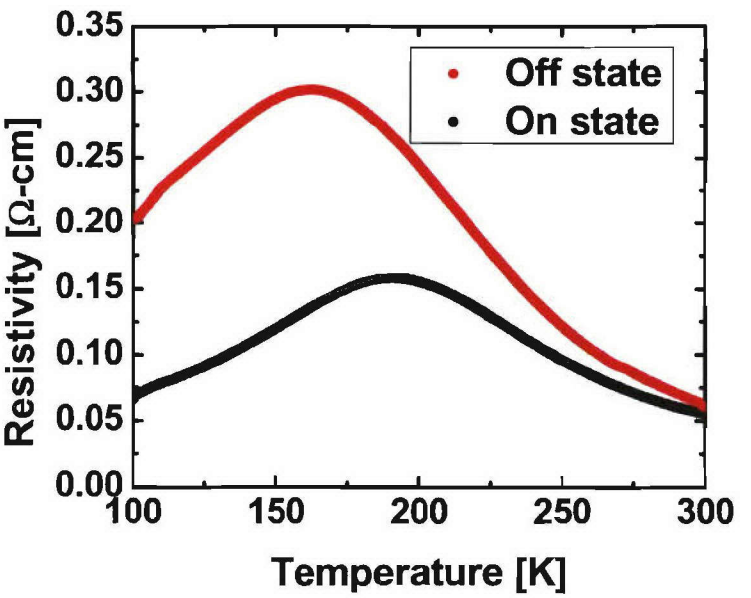

Figure 1: Resistivity as a function of temperature for a PZT/4 nm $La_{0.84}Sr_{0.16}MnO_3$ heterostructure for both polarization states of PZT.

Figure 2a shows the room temperature resistivity of a 4 nm LSCO layer as a series of bipolar 5 V pulses are applied (Fig. 2b). Resistance on/off ratios of 100 at 100K and

2.5 at room temperature were observed. Switching between the high resistivity off state and low resistivity on state was reversible.

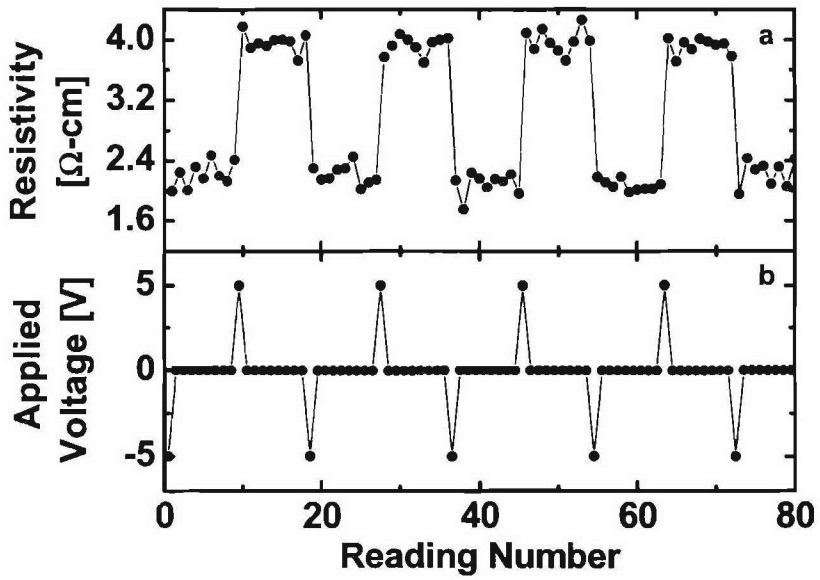

Figure 2: Room temperature resistivity of a PZT/4 nm $La_{0.70}Sr_{0.30}CoO_3$ heterostructure (upper figure) and the pulse sequence applied (lower figure).

The intrinsic switching time of ferroelectric domains is less than 1 ns, but for the fabricated devices, the switching times were longer due to the RC time constants of the devices. The switching time of single devices was determined by applying a sequence of 10 V pulses with durations ranging from 10 ns to 100 μs and measuring the change in resistance. For a 20 μm by 20 μm device, the switching time was found to be ~20 μs, in good agreement with the calculated RC time constant. The switching time was reduced to ~350 ns by using a more metallic material and scaling down the device size. We are currently investigating the use of e-beam lithography to reduce the device dimensions to length scales on the order of tens of nanometers, with a predicted switching time of less than one nanosecond. Also, we note that switching between the on and off states of current devices could be achieved by applying voltages as low as 2 volts, with the switching voltage being determined by the thickness of the ferroelectric. Future reduction in the thickness of the ferroelectric layer could reduce the switching voltage to tens of millivolts.

Characterization of device arrays:

A word line-bit line architecture (Fig. 3) with four devices was used to create arrays of independently addressable devices. Magnetotransport measurements were performed for both polarization states of PZT for the four devices in the array. For both polarization states, each of the four devices in the array showed similar values of resistivity, Curie temperature, on-off ratio, and magnetoresistance ratio, suggesting the film properties are uniform over millimeter length scales. By selectively applying voltage pulses to the word lines and bit lines, we were able to switch the state of one, two, three, or all four devices in the array without disturbing the other devices.

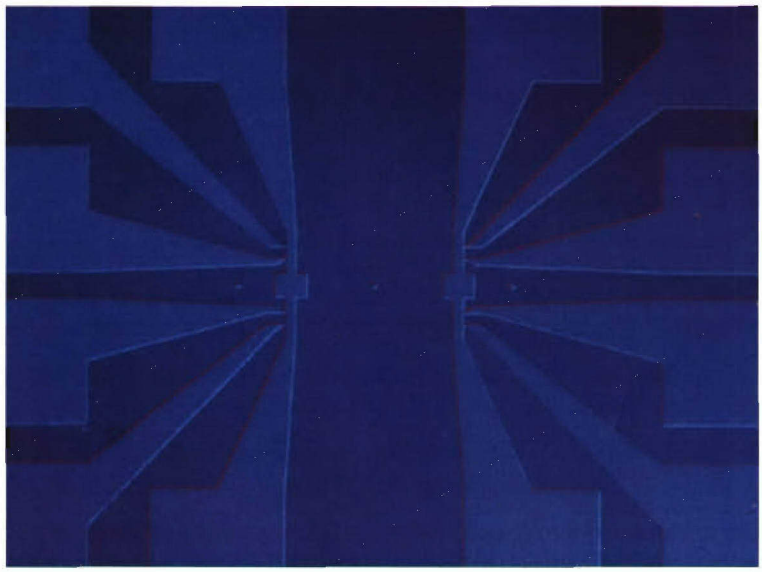

Figure 3: $SrTiO_3$ substrate after lithographic patterning for a four device array. The two bit lines run vertically. A second lithography step is required before deposition of the word lines and electrodes.

Integration with silicon

Incorporation into standard integrated circuits used in computer processors and other electronic devices is needed for the proposed device to have broad application. Most mainstream electronics today relies on silicon-based devices. We have been working on integrating single crystalline all-oxide epitaxial heterostructures on silicon through the growth of $SrTiO_3$ buffers. $SrTiO_3$ is an insulating perovskite oxide that is commonly used as the substrate for growing epitaxial oxide thin films.

We worked on a process to deposit crystalline $SrTiO_3$ layers on silicon without oxidizing the silicon surface. Preventing the formation of SiO_2 is critical since SiO_2 typically grows as an amorphous layer; such amorphous layers can prevent the growth

of epitaxial oxide structures on top. The technique we used involves forming a strontium-silicon transition layer, which reduces the oxygen affinity of the underlying silicon while maintaining crystal registry with it. This transition layer is needed as a chemical buffer because of the dissimilarity of the chemical properties of silicon and the $SrTiO_3$. The growth of this transition layer requires a high degree of thickness control, on the order of a tenth of a monolayer, necessitating the use a molecular beam epitaxy (MBE) system designed specifically for oxide growth.

Growth of the crystalline $SrTiO_3$ buffer on top of the transition layer entails a balance between kinetic and thermodynamic limitations of the system. We used the fact that $SrTiO_3$ is thermodynamically stable on silicon, as long as there is no excess oxygen (i.e., the silicon does not oxidize by removing oxygen from $SrTiO_3$). To ensure full oxidation of the $SrTiO_3$ layer, excess oxygen is used, but only at low temperatures (around room temperature), which kinetically prevents SiO_2 formation. To achieve crystallization of the $SrTiO_3$, high temperatures (~300°C) are used, but in the absence of excess oxygen. This alternation between kinetic and thermodynamic limits is needed to achieve epitaxial $SrTiO_3$ on silicon without the formation of SiO_2.

The thickness of the $SrTiO_3$ buffer was varied between 10 Å and 1000 Å, depending on the specific application. Once the $SrTiO_3$ buffer is formed, growth of other complex oxides is possible, and we have demonstrated the possibility of growing single layer ferroelectric PZT films on $SrTiO_3$ buffered silicon deposited at Yale. $SrTiO_3$ buffered silicon has also been used to grow other functional oxides, including the high-k dielectric $LaAlO_3$.

Future Directions:

Beyond the scope of the current work, we will continue to study the effects of device scaling on switching speed and switching voltage. In addition, we plan to focus on increasing the magnitude of the switching effect at room temperature, followed by additional characterization of device retention and ferroelectric fatigue effects. We will also investigate the use of $La_{1-x}Ba_xMnO_3$ and the electron-doped correlated oxide $La_{0.54}Sr_{0.46}MnO_3$ in future field effect devices. For the oxide-on-semiconductor project, we will characterize the spatial uniformity of the $SrTiO_3$ films. We are also working on growing other oxides, including $LaAlO_3$, on Si. Advanced Micro Devices is interested in continuing this research as part of their effort to fabricate next generation transistors that transcend the scaling limitations of mainstream semiconductor technologies.

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